

A: Amendment to the Detailed Description paragraph 26.

Delete paragraph 12 and move its contents to paragraph 14 such that the paragraph 14 is amended to read as follows:

[0014] The shortcomings of the prior art are overcome and additional advantages are provided through the provision of a mechanism that prohibits certain branches to be predicted in an asynchronous time frame in respect to the decoding of the said instruction. In particular, this modification is a descriptor bit in the opcode of a branch that states if the branch is allowed to be predicted or not. By allowing a bit within the instruction text to state if a particular instance of a branch is to be written into the BTB, two results are achieved: 1) branches which are performance critical and do not return from state altering routines can be added into the BTB for branch prediction. 2) Branches which exit a routing which altered the state of a machine can be blocked from being written into the BTB such that they are never predicted. This invention allows for higher processor performance via branch prediction while maintaining data integrity and preventing a measurable growth in silicon area or power.

Amend paragraph 26 to read as follows:

[0026] The resent invention is directed to a method and apparatus for branch prediction and branching in regard to selectively starting at decode 100, shown generally in Figure 1, where branches are to be classified as those branches which are predictable by the BHT/BTB 200 shown generally in Figure 2, and those branches which are not allowed to be predicted by the BHT/BTB 200. This method allows taking a set of brances which were previsouly not allowed to be prediced via the BTB/BTB, MCEND per example. The prohibition of the prior art was because certaine instances of predicting MCEND could lead to data integrity issues.